Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 7, 19, and 28, as follows:

Listing of Claims:

1. (Currently amended) A memory hub, comprising:

a reception interface operable to receive data words and to capture the data words in response to a first clock signal in a first time domain, and operable to provide groups of the captured data words on an output in response to a second clock signal in a second time domain, the second clock signal having a different clock frequency than the first clock signal;

a transmission interface coupled to the reception interface to receive the captured data words and operable to capture the data words in response to a third clock signal in the first time domain, and operable to provide the captured data words on an output; and

local control circuitry coupled to the output of the reception interface to receive the groups of data words, the local control circuitry operable to develop memory requests corresponding to the groups of data words.

2. (Original) The memory hub of claim 1 wherein the reception interface comprises:

a first input capture register having an input adapted to receive data words and having a clock input adapted to receive a first reception clock signal, the first input capture register capturing a data word on the input responsive to the first reception clock signal and applying the captured data word on an output;

a second input capture register having an input coupled to the input of the first input capture register and having a clock input adapted to receive a second reception clock

signal, the second input capture register capturing a data word on the input responsive to the second reception clock signal and applying the captured data word on an output;

a first storage buffer coupled to the output of the first input capture register and having a clock input adapted to receive a third reception clock signal, the first storage buffer storing sequentially captured data words on the output of the first input capture register;

a second storage buffer coupled to the output of the second input capture register and having a clock input adapted to receive a fourth reception clock signal, the second storage buffer sequentially storing captured data words on the output of the second input capture register;

a first multiplexer coupled to the first storage buffer to receive the stored data words and also coupled to the local control circuitry, the first multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry;

a second multiplexer coupled to the second storage buffer to receive the stored data words and also coupled to the local control circuitry, the second multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry; and

a capture read pointer circuit adapted to receive a fifth clock signal and being coupled to the first and second multiplexers, the capture read pointer operable to apply the selection signals to the multiplexers to supply the groups of captured data words in the buffers to the local control circuitry on a first-in-first-out basis.

3. (Original) The memory hub of claim 2 wherein the transmission interface comprises:

a first output capture register having an input coupled to the output of the first input capture register and having a clock input adapted to receive a first transmission clock signal, the first output capture register capturing a data word on the input responsive to the first transmission clock signal and applying the captured data word on an output; and

a second output capture register having an input coupled to the output of the second input capture register and having a clock input adapted to receive a second transmission

clock signal, the second output capture register capturing a data word on the input responsive to the second transmission clock signal and applying the captured data word on an output.

4. (Original) The memory hub of claim 1 wherein the reception interface further comprises optical interface circuitry adapted to receive optical signals corresponding to the data words and to convert the received optical signals into corresponding electrical signals.

5. (Original) The memory hub of claim 4 wherein the transmission interface further comprises optical interface circuitry that converts electrical signals corresponding to the data words into corresponding optical signals.

6. (Original) The memory hub of claim 1 wherein the memory hub further comprises:

an upstream reception port adapted to receive and capture upstream data words and operable to provide the captured data words to the local control circuitry; and

an upstream transmission port coupled to the local control circuitry to receive the upstream data words and operable to provide the upstream data words on an output.

7. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a reception interface operable to receive data words and to capture the data words in response to a first clock signal in a first time domain, and operable to provide groups of the captured data words on an output in response to a second clock signal in a second time domain, the second clock signal having a different clock frequency than the first clock signal;

a transmission interface coupled to the reception interface to receive the captured data words and operable to capture the data words in response to a third clock

signal in the first time domain, and operable to provide the captured data words on an output; and

local control circuitry coupled to the output of the reception interface to receive the groups of data words and also coupled to the memory devices, the local control circuitry operable to apply memory requests corresponding to the groups of data words to the memory devices to access memory cells in at least one of the memory devices responsive to at least some of the memory requests.

8. (Original) The memory module of claim 7 wherein the reception interface comprises:

a first input capture register having an input adapted to receive data words and having a clock input adapted to receive a first reception clock signal, the first input capture register capturing a data word on the input responsive to the first reception clock signal and applying the captured data word on an output;

a second input capture register having an input coupled to the input of the first input capture register and having a clock input adapted to receive a second reception clock signal, the second input capture register capturing a data word on the input responsive to the second reception clock signal and applying the captured data word on an output;

a first storage buffer coupled to the output of the first input capture register and having a clock input adapted to receive a third reception clock signal, the first storage buffer storing sequentially captured data words on the output of the first input capture register;

a second storage buffer coupled to the output of the second input capture register and having a clock input adapted to receive a fourth reception clock signal, the second storage buffer sequentially storing captured data words on the output of the second input capture register;

a first multiplexer coupled to the first storage buffer to receive the stored data words and also coupled to the local control circuitry, the first multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry;

a second multiplexer coupled to the second storage buffer to receive the stored data words and also coupled to the local control circuitry, the second multiplexer operable in

response to selection signals to apply groups of the captured data words to the local control circuitry; and

a capture read pointer circuit adapted to receive a fifth clock signal and being coupled to the first and second multiplexers, the capture read pointer operable to apply the selection signals to the multiplexers to supply the groups of captured data words in the buffers to the local control circuitry on a first-in-first-out basis.

9. (Original) The memory module of claim 8 wherein the transmission interface comprises:

a first output capture register having an input coupled to the output of the first input capture register and having a clock input adapted to receive a first transmission clock signal, the first output capture register capturing a data word on the input responsive to the first transmission clock signal and applying the captured data word on an output; and

a second output capture register having an input coupled to the output of the second input capture register and having a clock input adapted to receive a second transmission clock signal, the second output capture register capturing a data word on the input responsive to the second transmission clock signal and applying the captured data word on an output.

10. (Original) The memory module of claim 7 wherein the plurality of memory devices comprise SDRAMs.

11. (Original) The memory module of claim 7 wherein the memory hub further comprises:

an upstream reception port adapted to receive and capture upstream data words and operable to provide the captured data words to the local control circuitry; and

an upstream transmission port coupled to the local control circuitry to receive the upstream data words and operable to provide the upstream data words on an output.

12. (Original) The memory module of claim 7 wherein the reception interface further comprises optical interface circuitry adapted to receive optical signals corresponding to the data words and to convert the received optical signals into corresponding electrical signals.

13. (Original) The memory module of claim 12 wherein the transmission interface further comprises optical interface circuitry that converts electrical signals corresponding to the data words into corresponding optical signals.

14. (Original) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a physical reception port adapted to receive data words;

a bypass path coupled to the physical reception port;

a physical transmission port coupled to the bypass path; and

local control circuitry coupled to the physical reception port and to the plurality of memory devices.

15. (Original) The memory module of claim 14 wherein the physical reception port comprises:

a first input capture register having an input adapted to receive the data words, an output, and a clock input;

a second input capture register having an input coupled to the input of the first input capture register, an output, and a clocking input;

a first storage buffer coupled to the output of the first input capture register and having a clock input;

a second storage buffer coupled to the output of the second input capture register and having a clock input;

a first multiplexer coupled to the first storage buffer and coupled to the local control circuitry, and having selection inputs;

a second multiplexer coupled to the second storage buffer and coupled to the local control circuitry, and having selection inputs; and

a capture read pointer circuit coupled to the selection inputs of the first and second multiplexers.

16. (Original) The memory module of claim 15 wherein the physical transmission port comprises:

a first capture register having an input coupled to the bypass path, an output, and a clock input; and

a second capture register having an input coupled to the bypass path, an output, and a clock input.

17. (Original) The memory module of claim 14 wherein the bypass path comprises a plurality of conductive lines coupled between the physical reception and transmission ports.

18. (Original) The memory module of claim 14 wherein the memory hub further comprises an upstream transmission port and an upstream reception port coupled to the local control circuitry.

19. (Currently amended) A memory system, comprising:

a system controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed communications links, at least one of the memory modules being coupled to the system controller through a respective high-speed communications link, and each memory module comprising:

a plurality of memory devices;

a reception interface operable to receive data words from the corresponding high-speed communications link and to capture the data words in response

to a first clock signal in a first time domain, and operable to provide groups of the captured data words on an output in response to a second clock signal in a second time domain, the second clock signal having a different clock frequency than the first clock signal;

a transmission interface coupled to the reception interface to receive the captured data words and operable to capture the data words in response to a third clock signal in the first time domain, and operable to provide the captured data words on the corresponding high-speed communications link; and

local control circuitry coupled to the output of the reception interface to receive the groups of data words and also coupled to the memory devices, the local control circuitry operable to apply memory requests corresponding to the groups of data words to the memory devices to access memory cells in at least one of the memory devices responsive to at least some of the memory requests.

20. (Original) The memory system of claim 19 wherein each of the high-speed communications links comprises an optical communications link.

21. (Original) The memory system of claim 19 wherein the reception interface comprises:

a first input capture register having an input adapted to receive data words and having a clock input adapted to receive a first reception clock signal, the first input capture register capturing a data word on the input responsive to the first reception clock signal and applying the captured data word on an output;

a second input capture register having an input coupled to the input of the first input capture register and having a clock input adapted to receive a second reception clock signal, the second input capture register capturing a data word on the input responsive to the second reception clock signal and applying the captured data word on an output;

a first storage buffer coupled to the output of the first input capture register and having a clock input adapted to receive a third reception clock signal, the first storage buffer storing sequentially captured data words on the output of the first input capture register;

a second storage buffer coupled to the output of the second input capture register and having a clock input adapted to receive a fourth reception clock signal, the second storage buffer sequentially storing captured data words on the output of the second input capture register;

a first multiplexer coupled to the first storage buffer to receive the stored data words and also coupled to the local control circuitry, the first multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry;

a second multiplexer coupled to the second storage buffer to receive the stored data words and also coupled to the local control circuitry, the second multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry; and

a capture read pointer circuit adapted to receive a fifth clock signal and being coupled to the first and second multiplexers, the capture read pointer operable to apply the selection signals to the multiplexers to supply the groups of captured data words in the buffers to the local control circuitry on a first-in-first-out basis.

22. (Original) The memory system of claim 21 wherein the transmission interface comprises:

a first output capture register having an input coupled to the output of the first input capture register and having a clock input adapted to receive a first transmission clock signal, the first output capture register capturing a data word on the input responsive to the first transmission clock signal and applying the captured data word on an output; and

a second output capture register having an input coupled to the output of the second input capture register and having a clock input adapted to receive a second transmission clock signal, the second output capture register capturing a data word on the input responsive to the second transmission clock signal and applying the captured data word on an output.

23. (Original) The memory system of claim 19 wherein the plurality of memory devices comprise SDRAMs.

24. (Original) The memory system of claim 19 wherein the memory hub further comprises:

an upstream reception port adapted to receive and capture upstream data words and operable to provide the captured data words to the local control circuitry; and

an upstream transmission port coupled to the local control circuitry to receive the upstream data words and operable to provide the upstream data words on an output.

25. (Original) The memory system of claim 19 wherein the reception interface further comprises optical interface circuitry adapted to receive optical signals corresponding to the data words and to convert the received optical signals into corresponding electrical signals.

26. (Original) The memory system of claim 25 wherein the transmission interface further comprises optical interface circuitry that converts electrical signals corresponding to the data words into corresponding optical signals.

27. (Original) The memory system of claim 19 wherein the plurality of memory modules are coupled in a daisy-chain configuration with a first one of these memory modules being coupled to the system controller through the corresponding high-speed communications link.

28. (Currently amended) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed communications links, at least one of the memory modules being coupled to the system controller through a respective high-speed communications link, and each memory module comprising:

a plurality of memory devices;

a reception interface operable to receive data words from the corresponding high-speed communications link and to capture the data words in response to a first clock signal in a first time domain, and operable to provide groups of the captured data words on an output in response to a second clock signal in a second time domain, the second clock signal having a different clock frequency than the first clock signal;

a transmission interface coupled to the reception interface to receive the captured data words and operable to capture the data words in response to a third clock signal in the first time domain, and operable to provide the captured data words on the corresponding high-speed communications link; and

local control circuitry coupled to the output of the reception interface to receive the groups of data words and also coupled to the memory devices, the local control circuitry operable to apply memory requests corresponding to the groups of data words to the memory devices to access memory cells in at least one of the memory devices responsive to at least some of the memory requests.

29. (Original) The computer system of claim 28 wherein each of the high-speed communications links comprises an optical communications link.

30. (Original) The computer system of claim 28 wherein the reception interface comprises:

a first input capture register having an input adapted to receive data words and having a clock input adapted to receive a first reception clock signal, the first input capture register capturing a data word on the input responsive to the first reception clock signal and applying the captured data word on an output;

a second input capture register having an input coupled to the input of the first input capture register and having a clock input adapted to receive a second reception clock signal, the second input capture register capturing a data word on the input responsive to the second reception clock signal and applying the captured data word on an output;

a first storage buffer coupled to the output of the first input capture register and having a clock input adapted to receive a third reception clock signal, the first storage buffer storing sequentially captured data words on the output of the first input capture register;

a second storage buffer coupled to the output of the second input capture register and having a clock input adapted to receive a fourth reception clock signal, the second storage buffer sequentially storing captured data words on the output of the second input capture register;

a first multiplexer coupled to the first storage buffer to receive the stored data words and also coupled to the local control circuitry, the first multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry;

a second multiplexer coupled to the second storage buffer to receive the stored data words and also coupled to the local control circuitry, the second multiplexer operable in response to selection signals to apply groups of the captured data words to the local control circuitry; and

a capture read pointer circuit adapted to receive a fifth clock signal and being coupled to the first and second multiplexers, the capture read pointer operable to apply the selection signals to the multiplexers to supply the groups of captured data words in the buffers to the local control circuitry on a first-in-first-out basis.

31. (Original) The computer system of claim 30 wherein the transmission interface comprises:

a first output capture register having an input coupled to the output of the first input capture register and having a clock input adapted to receive a first transmission clock signal, the first output capture register capturing a data word on the input responsive to the first transmission clock signal and applying the captured data word on an output; and

a second output capture register having an input coupled to the output of the second input capture register and having a clock input adapted to receive a second transmission clock signal, the second output capture register capturing a data word on the input responsive to the second transmission clock signal and applying the captured data word on an output.

32. (Original) The computer system of claim 28 wherein the plurality of memory devices comprise SDRAMs.

33. (Original) The computer system of claim 28 wherein the memory hub further comprises:

an upstream reception port adapted to receive and capture upstream data words and operable to provide the captured data words to the local control circuitry; and

an upstream transmission port coupled to the local control circuitry to receive the upstream data words and operable to provide the upstream data words on an output.

34. (Original) The computer system of claim 28 wherein the reception interface further comprises optical interface circuitry adapted to receive optical signals corresponding to the data words and to convert the received optical signals into corresponding electrical signals.

35. (Original) The computer system of claim 34 wherein the transmission interface further comprises optical interface circuitry that converts electrical signals corresponding to the data words into corresponding optical signals.

36. (Original) The computer system of claim 28 wherein the plurality of memory modules are coupled in a daisy-chain configuration with a first one of these memory modules being coupled to the system controller through the corresponding high-speed communications link.

37. (Original) A method of processing downstream memory requests in a memory system including a plurality of memory hubs connected in a serial configuration, the method comprising:

receiving a data word at each memory hub;

latching each received data word in the memory hub responsive to a first clock signal in a first clock domain;

forwarding each latched data word to the next downstream memory hub responsive to a second clock signal in the first time domain; and

processing in each memory hub the latched data word responsive to a third clock signal in a second time domain, the second clock domain being defined by clock signals having rates lower than rates of clock signals in the first time domain.

38. (Original) The method of claim 37 wherein a plurality of data words comprises a memory request.

39. (Original) The method of claim 38 wherein the memory request comprises a read command.

40. (Original) The method of claim 37 wherein the second clock signal comprises a delayed version of the first clock signal.

41. (Original) The method of claim 37 wherein the clock signals in the first time domain have rates four times the rate of the third clock signal in the second time domain.

42. (Original) The method of claim 37 wherein the serial configuration comprises a plurality of memory hubs coupled in a daisy-chain configuration.

43. (Original) A method of processing downstream memory requests in a memory system including a plurality of memory hubs, the memory hubs being coupled in a daisy-chain configuration and the method comprising:

capturing downstream data words in each memory hub in a first clock domain;

bypassing each memory hub in the first clock domain to provide each captured downstream data word to a next adjacent downstream memory hub; and

processing in each memory hub the captured data word in a second clock domain being defined by clock signals having frequencies less than the frequencies of clock signals in the first clock domain.

44. (Original) The method of claim 43 wherein a plurality of data words comprises a memory request.

45. (Original) The method of claim 44 wherein the memory request comprises a read command.

46. (Original) The method of claim 43 wherein capturing downstream data words in each memory hub and bypassing each memory hub comprise capturing and bypassing responsive to first and second clock signals, respectively, and wherein the second clock signal comprises a delayed version of the first clock signal.

47. (Original) The method of claim 43 wherein the first time domain is defined by clock signals having frequencies four times the frequencies of clock signals in the second time domain.